

A high-speed analog-to-digital converter using Josephson self-gating-AND comparators

著者	Petersen D., Ko H., Jewett R., Nakajima K., Nandakumar V., Spargo J.
journal or publication title	IEEE Transactions on Magnetics
volume	21
number	2
page range	200-203
year	1985
URL	http://hdl.handle.net/10097/48234

A High-Speed Analog-to-Digital Converter Using Josephson Self-Gating-AND Comparators

D. A. Petersen, H. Ko, R. E. Jewett, K. Nakajima,
V. Nandakumar, J. W. Spargo, and T. Van Duzer

Department of Electrical Engineering and Computer Science
Electronics Research Laboratory
University of California
Berkeley, CA 94720

ABSTRACT

A Josephson Analog-to-Digital (A/D) converter which employs Self-Gating-AND (SGA) circuits as comparators has been designed and experimentally investigated. A functional description of the SGA is presented and the design of a four-bit A/D converter is described. High-speed measurements demonstrate four-bit quantization of 280 MHz sinusoidal inputs, and three-bit quantization of 499 MHz inputs at a 1.0 GHz conversion rate.

Introduction

The periodic threshold characteristic of a previously reported 1:2:1 split-fed three-junction superconducting quantum interference device (SQUID) is ideal for use in analog-to-digital conversion[1,2]. This paper will discuss an SGA comparator using this SQUID and will examine the most important feature of this circuit namely a very short aperture time. An A/D converter implemented using this comparator will be shown and experimental results presented.

The SGA Comparator

At the heart of a high-speed A/D converter are latching comparator circuits. Conventionally, comparators with a sin-

gle decision threshold are used, resulting in a total comparator count of $2^n - 1$, where n is the resolution in bits. The SGA[3] is a circuit that exploits the periodic characteristic of a SQUID to enable more thresholds per comparator, and hence fewer comparators per converter. An SGA is shown schematically in Fig. 1.

The SGA consists of two 1:2:1 SQUIDs and two current injection logic (CIL) gates[4] in a cross-coupled configuration. The analog input supplies current to the control line of S1 while the control line of S2 is fed by a dc reference current. The gate current to both S1 and S2 is a clock waveform with a fast rising edge. Before the clock rises, all Josephson junctions are in the superconducting state. As the clock current increases, the critical current of either S1 or S2 will be reached first, depending on the analog input at that time. This dependence is shown in Fig. 2. Here if the analog input is in any of the regions marked "1" the critical current of S1 will be reached first. If the analog input is in any of the regions marked "0" the critical current of S2 will be reached first. If the critical current of S1 is reached first, it switches to the voltage state, thus diverting current into C1 and out of C2. CIL circuits act as AND logic gates, switching to the voltage state only if both inputs have current flowing into them. This is now the case for C1, which then switches to the voltage state. This causes a break in the superconducting path from the gate of S2 to ground, thereby reducing the gate current of S2 and preventing it from switching. The result is ≈ 2 mV at the TRUE output port and zero voltage at the COMPLEMENT output port. In the case where the critical current of S2 is reached first, the situation is reversed and a positive voltage appears at the COMPLEMENT output port with zero voltage at the TRUE output port.

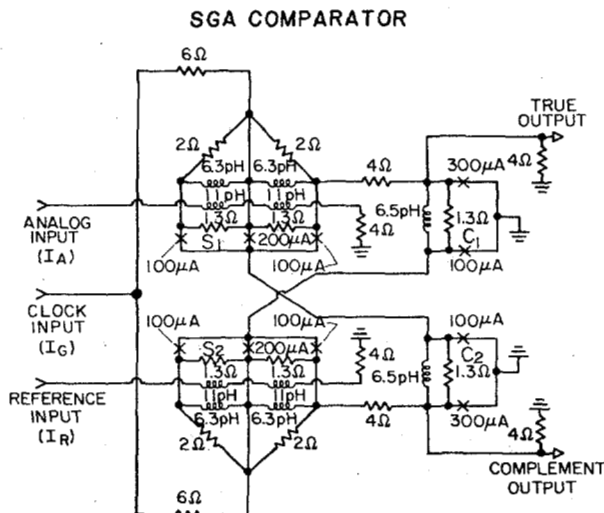


Fig. 1 Self-Gating-AND (SGA) Comparator Schematic Diagram.

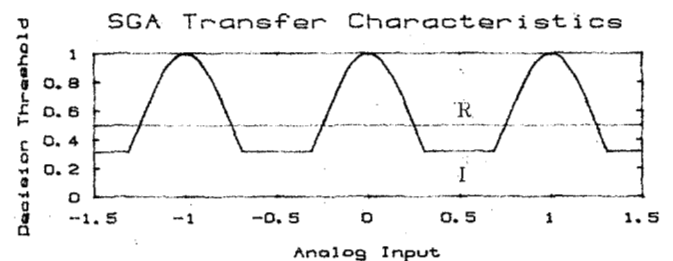


Fig. 2 SGA Input/Output Characteristic with Input and Reference SQUID Thresholds indicated.

Thus the SGA acts as a comparator with a periodic threshold characteristic. Notice that the SGA comparator evaluates the analog input only on the rising edge of the clock. This is due to simultaneous transfer of current from one CIL gate to the other when S1 or S2 switches and gives the circuit an

Manuscript received September 10, 1984.

Supported by the Office of Naval Research under contract number N00014-77-C-0419.

edge-triggered nature. Hence this circuit can quantize very fast-moving signals if the clock has a fast rising edge and device switching times are kept short.

An SGA-Based A/D Converter

The individual output bits of an A/D converter have a periodic dependence on the analog input to the converter. This dependence is the same as that of a single SGA comparator so an n -bit A/D converter can be made using only n SGA comparators, one for each bit[5]. This compares favorably to the 2^{n-1} comparators necessary in a conventional design. The number of periods used for a particular bit is a function of the significance of the bit.

Conventional A/D converters usually have a natural binary output scheme where the MSB goes through one complete cycle as the analog input goes from minimum (all zeros) to maximum (all ones). Each subsequent output bit contains twice as many cycles as its immediate superior with the LSB containing 2^{n-1} cycles for an n -bit converter. This sequence is shown in Fig. 3a. The difficulty in applying this scheme to an SGA type A/D converter is that transitions in output bits coincide. Small offset or gain errors in SGA characteristics would cause large conversion errors since changing the value of a single output bit at a point where transitions coincide can correspond to a digital value far from the desired value.

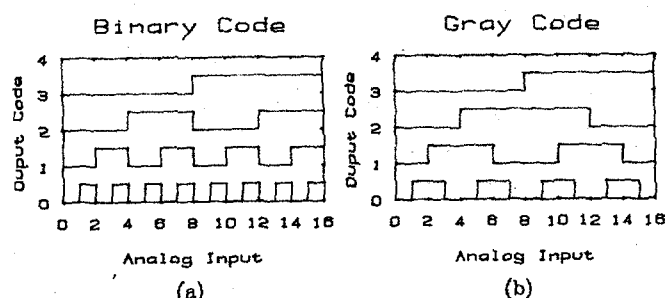


Fig. 3 A/D Converter Input/Output Sequences; (a) Natural Binary (b) Gray Code.

By shifting the output bit periods appropriately, a sequence can be obtained that avoids any coincident transitions. This results in a Gray-coded output sequence as the analog input goes from minimum to maximum value as shown in Fig. 3b. The salient feature of a Gray code sequence is that only one bit changes at a time, thereby eliminating the problem of large errors in close proximity to a decision threshold.

To achieve the appropriate relationship between the n bits of an A/D converter, the analog signal is fed into a binary resistive divider producing n outputs. The amplitude of each output is half that of its immediate superior. The largest signal is fed into the LSB SGA causing it to cover 2^{n-2} cycles. The smallest signal is fed into the MSB SGA causing it to cover $\frac{1}{2}$ cycle. This naturally arranges the output cycles into a Gray code sequence.

All results presented in the testing section of this paper use this Gray code scheme. If natural binary output code is desired, additional combinational logic circuitry can be included[6, 7].

High-Speed Considerations

In order to achieve high-speed quantization of fast-moving inputs, several additional constraints are placed on the converter design. An important constraint is the aperture time of the basic comparator elements. Aperture time is the window in time over which the analog input is evaluated. If the input

moves across more than one quantization level during this time the LSB(s) of the conversion may be in error. Alternatively, analog input bandwidth determines the maximum full amplitude sinusoidal input that can be accurately quantized to full resolution. Aperture time τ_{ap} and analog input bandwidth BW_i are related for a given resolution by

$$\tau_{ap} = \frac{1}{2^n \pi BW_i}$$

For a four-bit A/D converter with $BW_i = 500$ MHz, $\tau_{ap} \approx 40$ ps.

Another consideration is the problem of signal/clock synchronism. The comparator elements must all evaluate the input simultaneously. Small on-chip delays on the order of τ_{ap} will cause errors in the LSB(s). The solution is to match the delays in clock and signal path to each comparator element. This can be of considerable difficulty in conventional A/D converters with the large number of comparator elements involved. This problem is avoided by the SGA A/D converter due to reduced comparators count. Another advantage of the low comparator count is that input capacitance is minimized, easing the difficulty of driving the input with high frequency signals.

Test System

A four-bit A/D converter was fabricated using a standard Pb-alloy process. A block diagram of the chip layout is shown in Fig. 4. In order to demonstrate a high sampling rate and short aperture time, a primary set of SGA comparators is clocked with a 1.0 GHz sine wave. Following this is an identical set of SGA comparators that act as latches. These secondary latches are clocked with a divided version of the primary clock yielding at their output one conversion result out of every N (N is 32 or 64 in all results presented here). This testing scheme fully exercises the converter while avoiding the difficulty of processing outputs at one gigasample/second with room temperature electronics.

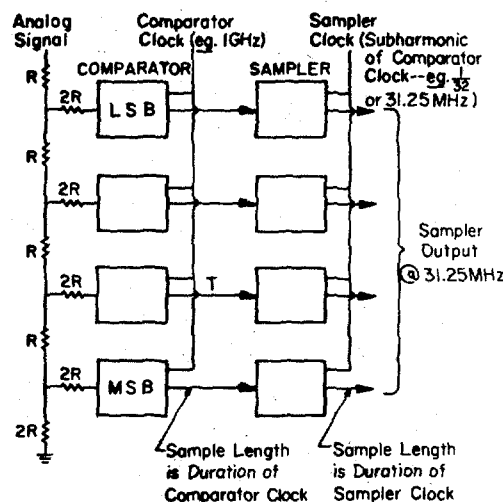


Fig. 4 Four-Bit Josephson A/D Converter Block Diagram with Resistive Divider Network, and Output Latches Shown.

As shown in Fig. 5, the testing system consists of an analog signal source, a 1.0 GHz clock source to establish the sampling rate, a division circuit to provide the secondary clock, and a waveform reconstruction circuit. Note that for each of the three high frequency inputs, a complementary version is generated and transmitted to the chip. These complement signals are terminated to the chip ground plane to provide cancellation of unwanted interference due to common ground induc-

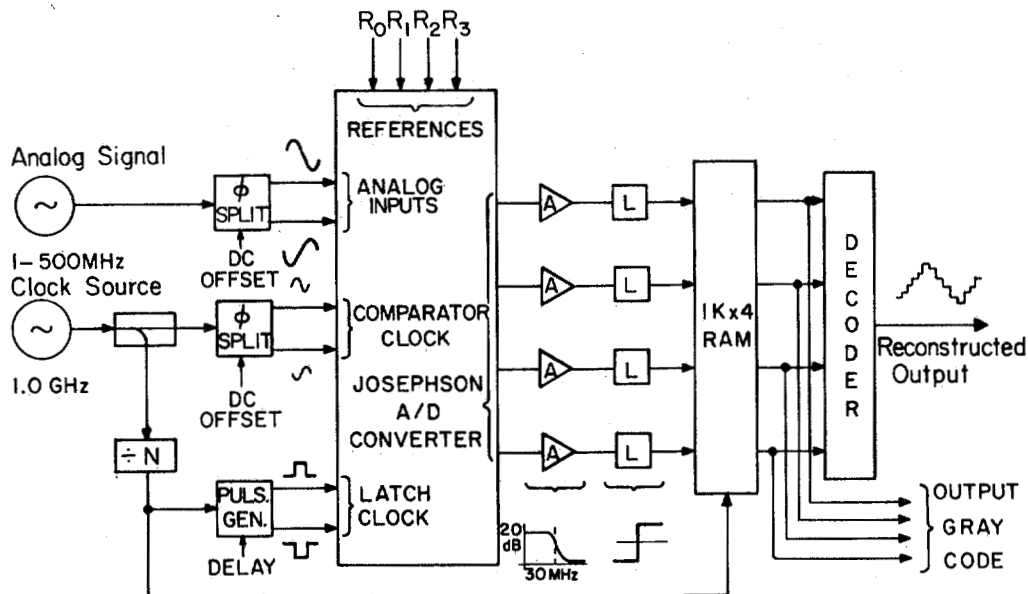


Fig. 5 A/D Converter Test System.

tance present in our chip holder.

Following conversion, the output bits are processed with a bank of amplifier/limiters. The amplifiers provide signal gain and limit the bandwidth to reduce errors due to out-of-band noise. The limiters have an adjustable decision level enabling accurate reception of the output bits. The resulting parallel data sequence is stored in a cyclically addressed RAM circuit allowing analysis of a large number of samples. The output from the RAM is decoded from Gray code into natural binary and converted back to a multi-level analog form with a digital-to-analog converter.

To determine the analog input bandwidth of the converter, a beat frequency test was performed. This test consists of sampling a sinusoid of frequency $(Mf_s/N) \pm \Delta f$ where f_s is the primary sampling rate, N is the division integer, M is a multiplying integer and Δf is a small frequency offset. The result of sampling this input is a relatively low frequency beat between the input and the secondary clock rate. This beat has a frequency of Δf Hz. For example $N = 32$, $M = 9$, $f_s = 1.0$ GHz and $\Delta f = 1.0$ MHz yields an input frequency of 280.25 MHz. This input is sampled about 3.5 times per cycle with every 32nd sample being latched and brought out of the dewar. These samples trace out the input sinusoid with a 1.0 MHz repetition rate.

Experimental Results

A four-bit converter was tested for functionality at a clock rate of 1.0 GHz with $N = 64$, resulting in approximately 16 megasamples per second. The input frequency was 1.0 MHz. Figure 6 shows the resulting Gray-coded output bits along with the reconstructed waveform. The reconstruction is monotonic, thus demonstrating good alignment and periodicity of all output bits. This verifies operation of all four input SGA comparators at a high conversion rate and also demonstrates working output latches.

To measure input bandwidth the beat frequency test described in the previous section was performed. Here the clock remains at 1.0 GHz with $N = 32$ yielding 31.25 megasamples per second. An analog input frequency of 280.25 MHz was

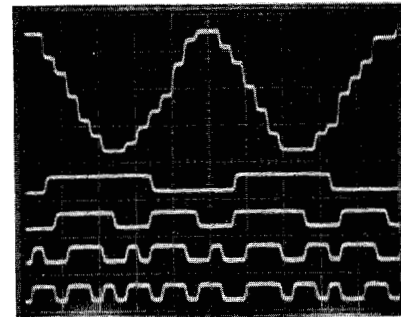


Fig. 6 Quantization of a Sine Wave, (trace 1) Reconstructed Waveform, (traces 2-5) Gray-Coded outputs MSB to LSB respectively. Input = 1.0 MHz, Conversion Rate = 1.0 GHz, $N=64$.

used giving a low frequency beat of 1.0 MHz between the divided clock and the analog input. The result, shown in Fig. 7, is for a chip different from the one used to obtain Fig. 6. The output bit patterns, though qualitatively correct do not decode to a monotonic waveform. We believe this is due to a flaw in the resistive divider network used to distribute signal to the four SGA's. Also notice an error in the second MSB pattern. This and others like it were not stationary in the output pattern and are due to noise in the measurement.

To verify that the nonmonotonicity is due to fabrication defects and not to high frequency effects, a low frequency input was quantized. Shown in Fig. 8 is the output with a 500 kHz analog input. A symmetrical nonmonotonic sequence the same as that of the 280.25 MHz result is present. This indicates that the four comparators are performing the same up to 280.25 MHz.

Theoretically, as input frequency is increased resolution will decrease as the LSBs fail to operate. A measurement of this effect is shown in Fig. 9 where the analog input frequency

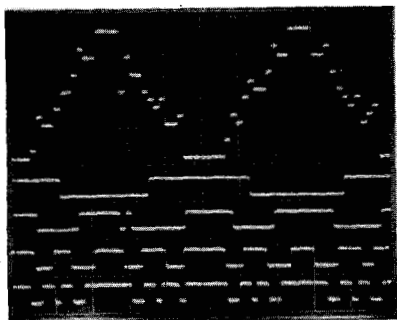


Fig. 7 Quantization of a Sine Wave, (trace 1) Reconstructed Waveform, (traces 2-5) Gray-Coded outputs MSB to LSB respectively. Input = 280.25 MHz, Conversion Rate = 1.0 GHz, $N=32$.



Fig. 8 Quantization of a Sine Wave, (trace 1) Reconstructed Waveform, (traces 2-5) Gray-Coded outputs MSB to LSB respectively. Input = 500 kHz, Conversion Rate = 1.0 GHz, $N=32$.

is 499 MHz. Here the LSB no longer shows the same bit pattern as for lower frequency inputs. As mentioned in a previous section, input bandwidth is proportional to clock risetime. Here we are using a sinusoidal clock with a relatively slow risetime of ≈ 350 ps. It is unclear at this time whether input bandwidth is limited by clock risetime or if dynamic effects in the SGA itself are dominant.

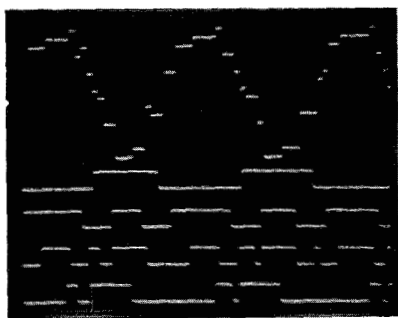


Fig. 9 Quantization of a Sine Wave, (trace 1) Reconstructed Waveform, (traces 2-5) Gray-Coded outputs MSB to LSB respectively. Input = 499 MHz, Conversion Rate = 1.0 GHz, $N=32$.

Conclusion

We have designed, fabricated, and tested four-bit A/D converters using SGA circuits as latching comparator elements. These circuits have been tested with high frequency inputs at

conversion rates of one gigasample/second. These results represent first attempts and are therefore preliminary. With improvements in our testing apparatus and refinements in our design we expect to increase the resolution, conversion rate and analog input bandwidth of our converter.

References

1. S. H. Dhong, R. E. Jewett, J. W. Spargo, and T. Van Duzer, "A Symmetrical Three-Junction Superconducting Quantum Interference Device," *J. Appl. Phys.*, vol. 54 (1), January 1983.
2. R. E. Harris, C. A. Hamilton, and F. L. Lloyd, "Multiple-Quantum Interference Superconducting Analog-to-Digital Converter," *Appl. Phys. Lett.*, vol. 35, pp. 720-721, November 1979.
3. A. Davidson, "A Josephson Latch," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 583-587, October 1978.
4. T. R. Gheewala, "A 30-ps Josephson Current-Injection Logic (CIL)," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 787-793, October 1979.
5. S. H. Dhong, R. E. Jewett, and T. Van Duzer, "Josephson Analog-to-Digital Converter Using Self-Gating-AND Circuits as Comparators," *IEEE Trans. Magn.*, vol. MAG-19, pp. 1282-1285, May 1983.
6. J. W. Spargo, R. E. Jewett, and T. Van Duzer, "A Pipelined Gray Code-to-Natural Binary Decoder for Use in a Josephson A/D Converter," *IEEE Trans. Magn.*, vol. MAG-19, pp. 1255-1258, May 1983.
7. J. W. Spargo, "A Pipelined Gray Code-to-Natural Binary Decoder for Use in a Josephson A/D Converter," *Ph. D. Dissertation, EECS, University of California, Berkeley*, September, 1983.